An Embedded Transmission Line Micro-Ball Grid Array X-Band Power Amplifier

Thomas Budka[+], Leon Stiborek, Lonny Heinrich and Cary Kyhl

Raytheon TI Systems, P.O. Box 655474, MS 217, Dallas, Texas 75265-5474

[+]now with M/A-COM Corp. R&D, P.O. Box 3295, Lowell, MA 01853-3295

Abstract

This paper describes an electronic packaging topology using embedded transmission line (ETL) monolithic microwave integrated circuits (MMIC) that have been flip-chip mounted on a beryllia (BeO) micro-ball grid array (µBGA) ceramic carrier with a z-axis interconnect material. Small signal S-parameters are presented at each stage during the assembly process and negligible frequency shifts are observed due to the flip-chip packaging before and after encapsulation. Increased gains of 2.0 dB with the unencapsulated and 2.2 dB with the encapsulated packaged part are observed compared to the on-wafer measurements at 10 GHz under the same bias conditions.

Introduction

Embedded transmission line (ETL) flip-chip packages offer a host of benefits such as low interconnect and FET source inductances as well as low thermal impedance from the active device to its heat sink. Low interconnect inductances enable high frequency connections from the chip to the package and from the package to the intended host board. Direct metal connections from the active FET area surface to a high thermal conductivity carrier greatly reduce the thermal impedance of gallium arsenide (GaAs) power amplifiers compared to FETs on 100µm thick GaAs substrates. This reduction improves reliability and electrical performance.

The multilayer packaging approach presented in this paper is based on the use of ETL MMICs combined with a micro-ball grid array substrate mounted on a ceramic test fixture. The ETL MMIC structure, first described in [1], differs from standard MMICs in that the GaAs substrate is not thinned (635µm) and acts primarily as a cover to protect the ETL MMIC. Polyimide layers are patterned with metal lines and filled gold vias ending with a ground plane and signal pads.

ETL MMICs

Figure 1 displays a cross-section of several key ETL MMIC elements: FET, shunt capacitor and an inverted microstrip transmission. Models for these components have been developed under the MAFET Thrust 2 program and several are described in reference [2].

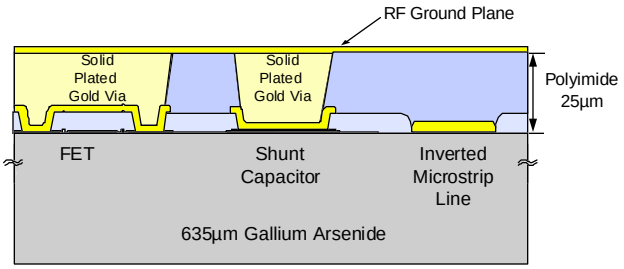


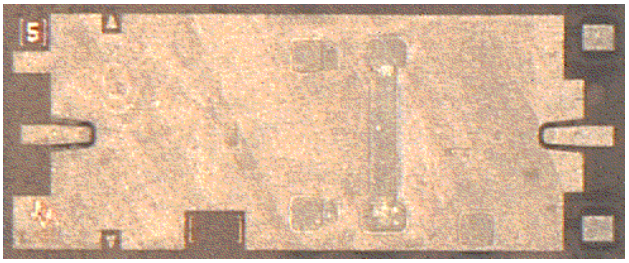
Figure 1. Basic ETL MMIC structure for a FET, shunt capacitor and inverted microstrip transmission line.

Figure 2a displays a photograph of the top side of the single stage ETL MMIC amplifier used in this demonstration along with the layout of the amplifier displayed in fig. 2b. The results from this chip were first described in [3] with a wirebonded module package. The µBGA package described in this paper along with the

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

encapsulation represent a new style of ETL MMIC package.

a)



b)

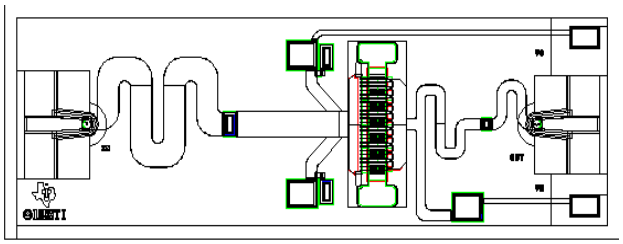


Figure 2. a) Photograph and b) layout of a one Watt single stage ETL amplifier at 11.5 GHz. Chip size is 3.03mm x 0.96mm.

One important consideration during the development of flip-chip MMICs is the ability to perform on-wafer RF probe measurements before and after mounting as well as provide a producible interconnect to the carrier [3]. In addition to the RF probe interface at the chip level, the next RF probe interface chosen for this particular design is at the µBGA test fixture level. Figure 3 displays an ETL MMIC mounted with a novel Z-axis material developed by Raytheon TI Systems (described in [3]) on a BeO ceramic carrier with silver epoxy attached 100pF capacitors above and below the ETL MMIC. Figure 4 displays a side view of the unencapsulated assembly with the 10mil diameter solder balls being visible between the package and the larger test fixture at the bottom. Figure 5 displays the encapsulated package from figure 4. A coplanar waveguide launch is selected so that the package can be measured with the same RF probes that were used for the chip-level test. In this paper a Line-Reflect-Match (LRM) calibration is used for all S-parameter measurements.

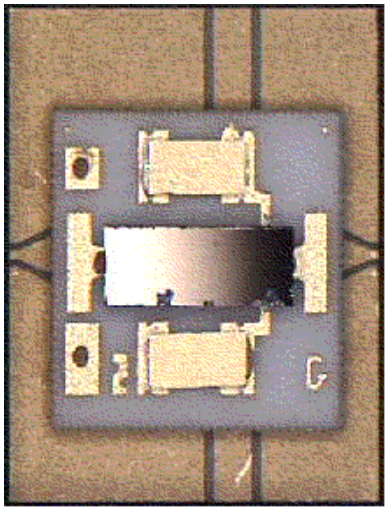


Figure 3. ETL MMIC flip chip assembly showing an ETL MMIC (center) with two flip chip capacitors on each side of the MMIC on a 20 mil thick BeO carrier.

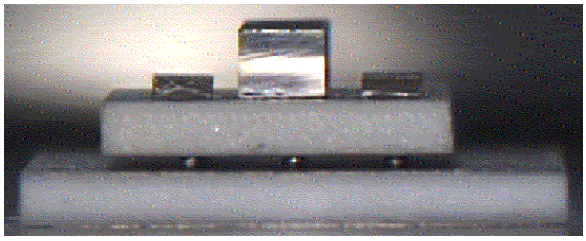


Figure 4. ETL MMIC µBGA flip-chip assembly (side view of figure 3).

ETL MMICs have a significant advantage compared to CPW flip-chip MMICs: their frequency response does not change appreciably when the chip is mounted or encapsulated because the MMIC is already shielded with a ground plane [3]. Figures 6a-d display the small signal S-parameters of the same ETL MMIC in wafer form, packaged form with and without chip encapsulation. The bias conditions were a drain voltage of 5V and a drain current of 90mA with a gate voltage of -0.9V.

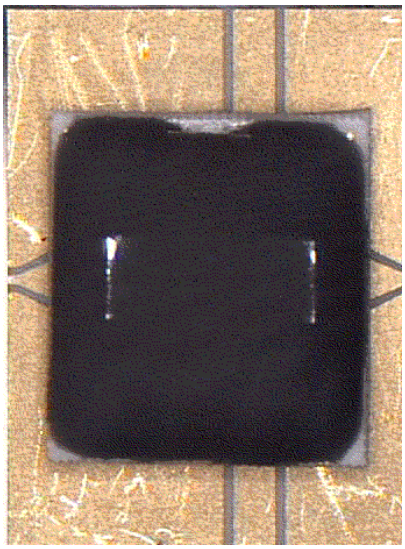
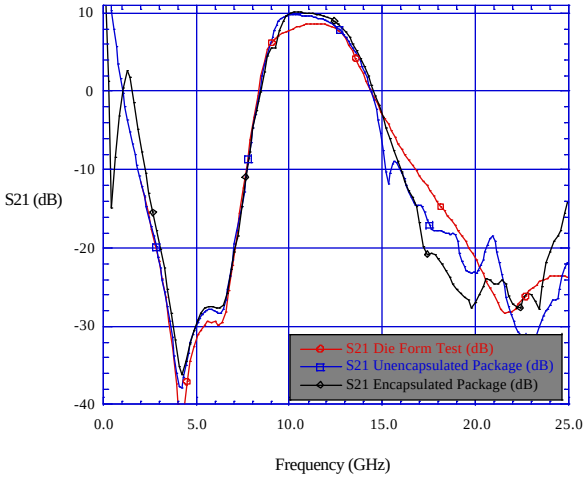
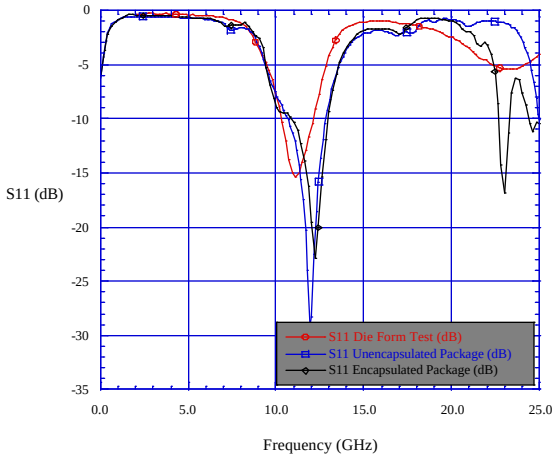


Figure 5. Encapsulated ETL MMIC µBGA flip-chip assembly from figure 4. RF input is at the left and the RF output is at the right.

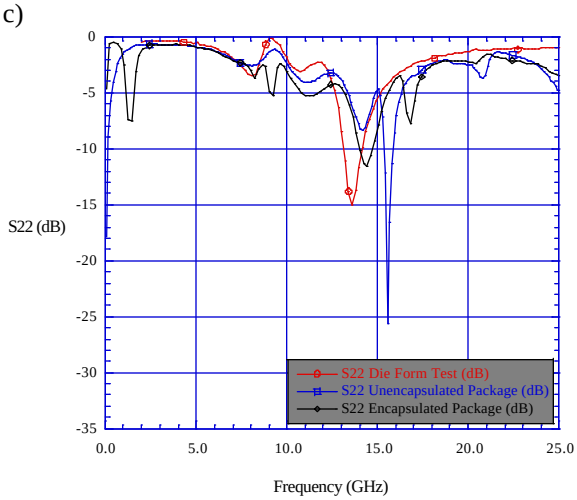
a)



b)



c)



d)

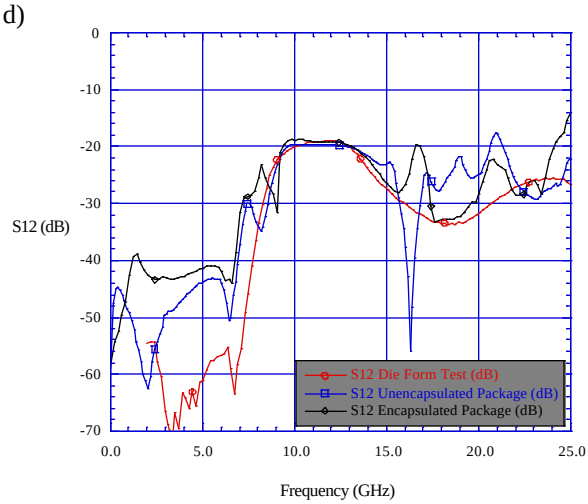


Figure 6. Small signal a) S_{21} b) S_{11} c) S_{22} and d) S_{12} of the same single stage X-band ETL amplifier in die form, unencapsulated package form and encapsulated package form.

As displayed in figure 6a, the small signal gain of the packaged ETL MMIC is observed to be greater than the on-wafer measured gain by as much at 2.0 dB at 10.0 GHz for the unencapsulated package and as much as 2.2 dB for the encapsulated package. This increase in small signal gain is most likely due to the improved thermal impedance of the flipped ETL MMIC compared to an upright ETL MMIC. Even though the small signal gain improved after packaging there were no observed frequency shifts in the ETL MMIC response before or after encapsulation.

In figure 6b, the return loss of the packaged unencapsulated and encapsulated ETL MMIC show improvements compared to the on-wafer measurements.

This can mainly be explained by the addition of interconnects and losses due to the feed networks that have now been included in the measurements and improved the return loss of the system. This particular package has not yet been subjected to environmental testing. However, bare ETL pHEMT die and passive Z-axis interconnect test structures have survived over 1000 temperature cycles from -55C to 125C.

The output power of this package (including test fixture losses) is measured to be 28dBm with 8dB large signal gain under 1dB compression and a power added efficiency (PAE) of 28% at 11.5 GHz. These results are slightly lower than the same MMIC in the package configuration from [2] where the BeO chip carrier is mounted directly to a heat sink using silver epoxy. The output power of the directly mounted ETL MMIC package from [2] was measured to be 29.4dBm with 23dBm input power under 3dB compression with 26.6% PAE. The lower output power of the µBGA package (approximately 2dBm) is most likely due to the higher thermal impedance of the µBGA package compared to same package with a large area attached directly to a heat sink.

Conclusions

The µBGA ETL package presented in this paper demonstrates minimal frequency shifts due to package mounting or package encapsulation. This important feature eliminates the need for corrected circuit simulations and multiple iterations due to unexpected shifts in the frequency response due to packaging effects of an encapsulated standard microstrip based MMIC or CPW flip-chip mounted MMIC. In addition, a wide variety of encapsulants may be used without regard to the high frequency dielectric properties in the configuration presented in this paper. Further packaging advances with ETL MMICs appear promising and producible within the next several years.

Acknowledgments

This work was funded by the Electronics Technology Office (ETO), Defense Advanced Research Projects Agency (DARPA) under the MAFET Thrust 2 program contract N00600-95-C-2889. The DARPA program manager is Lisa Sobolewski. The contract is administered by Glenn Marshall at NAWC-AD. The authors would like to thank Phyllis Aldert, Billy Ables, Gailon Brehm, Andrew Ketterson, Robert Peterson, Brit Potter, John Reddick, Hua-Quen Tserng and Karl Worthen for many helpful technical discussions.

References

1. H. Tserng, P. Saunier, A. Ketterson, L. Witkowski, T. Jones, “Embedded Transmission Line (ETL) MMIC for Low-Cost, High-Density Wireless Communication Applications,” IEEE Radio Freq. Integrated Circuits Symposium, pp. 41-44, 1997.

2. B. Heimer, T. Budka, “A Methodology for Modeling ETL MMIC Bends and Power Shunt Capacitor Components,” submitted for review to the 1998 IEEE MTT-S, November 1997.

3. T. Budka, A. Ketterson, H. Tserng, L. Stiborek, L. Heinrich, R. Smith, B. Ables, C. Kyhl, K. Worthen, G. Brehm and J. Reddick, “Embedded Transmission Line MMIC 1 Watt Flip Chip Assembly Using a Z-Axis Interconnect,” submitted for review to the IEEE Microwave and Guided Wave Letters, October 1997.